EXHIBIT A

PARTIES' JOINT CLAIM CONSTRUCTION CHART

FOR FAMILY 6 PATENTS

Disputed Claim Term	**Patent, Asserted Claims**	**Plaintiff's Proposed Construction**	**Defendants' Proposed Construction**
"transceiver"	'835 patent, claims 8, 10	"communications device capable of transmitting and receiving data wherein the transmitter portion and receiver portion share at least some common circuitry" Intrinsic Evidence: Ex. B ('835 patent) at Fig. 1, Fig. 2, 5:7-10, 7:67 – 8: 20.[1]	"communications device capable of transmitting and receiving data" Intrinsic Evidence *See, e.g.*, '835 at Abstract; 3:28-31; 4:32-36; 5:7-10; 7:67-8:8.[2]
"flag signal"	'835 patent, claims 8, 10	"inverted sync symbol or sync flag used to synchronize the switch to using an updated FIP setting" Intrinsic Evidence: Ex. B ('835 patent) at 11:4-9, 11:66 – 12:37.	"signal indicating when updated FIP settings are to be used" Intrinsic Evidence *See, e.g.*, '835 at 11:66-12:5; 12:25-37; 19:15-22; Fig. 6.
"flag signal"	'162 patent, claims 8, 9	"inverted sync symbol or sync flag used to synchronize the change to using an updated interleaver parameter value" Intrinsic Evidence: Ex. B ('835 patent) at 11:4-9, 11:66 – 12:37.	ADTRAN's Proposal: "signal indicating when an updated interleaver parameter value is to be used" Intrinsic Evidence *See, e.g.*, '162 at 12:1-7; 12:25-37; 19:14-21; Fig. 6.[3]

[1] The '835, and '162 patents share a common disclosure. For brevity, this document cites only to the '835 patent.
[2] Defendants citations are to US Patent No. 8,462,835 (Ex. B)
[3] Defendant ADTRAN's citations are to US Patent No. 8,594,162 (Ex. C)

Disputed Claim Term	**Patent, Asserted Claims**	**Plaintiff's Proposed Construction**	**Defendants' Proposed Construction**
"interleaver parameter value"	'835 patent, claim 10 '162 Patent, claim 8	"numerical value of an interleaver depth parameter" <u>Intrinsic Evidence:</u> Ex. B ('835 patent) at 1:60 – 2:33, 3:37-47, 12:40-64, 13:16-37, 13:43-53; Ex. D (U.S. Prov. Appl. No. 60/549804) at p. 18; Ex. E (ITU-T G.992.3 (7/2002)) at § 7.5, § 7.7.1.4, and § 7.7.1.5.	"the numerical value of the interleaver depth in number of codewords" <u>Intrinsic Evidence</u> *See, e.g.*, '835 at 2:2-15; 2:22-25. *See, e.g.*, '162 at 2:4-12; 2:20-23.
"FIP setting"	'835 patent, claims 8, 10	"set including at least one forward error correction parameter value and at least one interleaver parameter value" <u>Intrinsic Evidence:</u> Ex. B ('835 patent) at 1:60 – 2:33, 3:37-47, 12:40-64, 13:16-37, 13:43-53; Ex. D (U.S. Prov. Appl. No. 60/549804) at p. 18; Ex. E (ITU-T G.992.3 (7/2002)) at § 7.5, § 7.7.1.4, and § 7.7.1.5.	"forward error correction and interleaver parameters characterized by the set of parameters for codeword size in bytes, number of information bytes in a codeword, number of parity or redundancy bytes in a codeword, and interleaver depth in number of codewords" <u>Intrinsic Evidence</u> *See, e.g.*, '835 at Abstract; 2:11-15; 2:22-25; 3:37-47; 12:39-50; 13:15-28; 13:43-45.

Disputed Claim Term	**Patent, Asserted Claims**	**Plaintiff's Proposed Construction**	**Defendants' Proposed Construction**
"FIP value"	'835 patent, claims 8, 10	"numerical value of a forward error correction parameter or numerical value of an interleaver parameter" Intrinsic Evidence: Ex. B ('835 patent) at 1:60 – 2:33, 3:37-47, 12:40-64, 13:16-37, 13:43-53; Ex. D (U.S. Prov. Appl. No. 60/549804) at p. 18; Ex. E (ITU-T G.992.3 (7/2002)) at § 7.5, § 7.7.1.4, and § 7.7.1.5.	"numerical value of codeword size in bytes, number of information bytes in a codeword, number of parity or redundancy bytes in a codeword, or interleaver depth in number of codewords" Intrinsic Evidence *See, e.g.*, '835 at 2:11-15; 3:62-66; 9:61-10:4.
"the switching occurs on a pre-defined forward error correction codeword boundary"	'835 patent, claims 8, 10	"the switching to an updated FIP setting is effective on the boundary of a forward error correction codeword where the position of the boundary of each codeword is known prior to the switching" Intrinsic Evidence: Ex. B ('835 patent) at Fig. 3, Fig. 4, Fig. 6, 8:66 – 9:4, 9:23-29, 11:4-9, 11:66 – 12:37, 18:3-26, 19:14-30.	Indefinite
"the second interleaver parameter value is used for transmission on a pre-defined forward error correction codeword boundary"	'162 Patent, claim 8	"the second interleaver parameter value is used for transmission starting on a boundary of a forward error correction codeword where the position of the boundary of each codeword is known prior to use of the second interleaver parameter value"	ADTRAN's Proposal: Indefinite

Disputed Claim Term	**Patent, Asserted Claims**	**Plaintiff's Proposed Construction**	**Defendants' Proposed Construction**
		<u>Intrinsic Evidence:</u> Ex. B ('835 patent) at Fig. 3, Fig. 4, Fig. 6, 8:66 – 9:4, 9:23-29, 11:4-9, 11:66 – 12:37, 18:3-26, 19:14-30.	

Claim Term	Patent, Claims	Agreed Construction
Preamble	’835 patent, claims 8, 10	Parties agree that the preamble is limiting.
“steady state”	’835 patent, claims 8, 10	“the state of the transceiver reached after all initialization and training is completed in which user data is transmitted or received”